AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0070] of the specification as follows:

[0070] This way, source and drain regions 73a, 73b (FIG. 19), which are heavily doped with n-type impurity ions, are formed within the p-type wells 62a, 62b. Thus, two n-p-n type (NMOS) transistors 100, 200 ~~(FIG. 19)~~ are formed of the gate stacks 70a, 70b and their respective n-type source/drain regions 73a, 73b within the p-type wells 62a, 62b. As explained in more detail below and with reference to FIG. 20, the first NMOS transistor 100 formed in the memory array area is a fully-depleted (FD) SOI NMOS transistor with a p+ gate electrode, as opposed to a conventional n+ gate electrode. The p+ gate electrode with low channel doping ensures the fully-depleted mode for the access SOI NMOS transistor 100 in the memory array. The second NMOS transistor 200 formed in the periphery area is a partially-depleted, and not fully-depleted, SOI NMOS transistor. Thus, a fully-depleted and a partially-depleted MOSFET devices of the same conductivity type are formed on the same SOI substrate and without the conventional silicon thinning of the silicon layer of the prior art to obtain a fully-depleted device.